IN THE CLAIMS:

1. (Original) A method for precisely etching a wide bandgap semiconductor device, the method comprising the steps of:

(a) providing a multi-layer laminate including at least a first and second layer of wide bandgap semiconductor material;

(b) isolating an area of the first layer of semiconductor material for locating a conductance measurement device;

(c) measuring a first conductance of the isolated area of the first layer of semiconductor material using the conductance measurement device;

(d) first etching a first amount of the first layer of semiconductor material;

(e) measuring a second conductance of the isolated area of the first layer of semiconductor material subsequent to etching the first amount of the first layer of semiconductor material; and

(f) utilizing the first and second measured conductance to determine a time required to etch a second amount of the first layer of semiconductor material.

2. (Original) The method of Claim 1 the method comprising:

repeating steps (d) through (f) to determine an optimal time to etch the second amount of the first layer of semiconductor material to achieve a desired etch depth.

3. (Original) The method of Claim 1 the method comprising:

subsequent to the utilizing step, second etching the first layer of semiconductor material for the determined amount of time to remove the second amount of the first layer of semiconductor material.

4. (Original) The method of Claim 3 wherein the second etching step comprises:

etching at least a portion of the first layer of semiconductor material to a junction between the first and second layer of semiconductor material.

5. (Original) The method of Claim 3 wherein the second etching step comprises:

removing at least a portion of the first layer of semiconductor material to achieve a predetermined thickness of the at least a portion of the first layer of semiconductor material.

6. (Original) The method of Claim 1 wherein the utilizing step includes:

determining a difference between the first measured conductance and the second measured conductance; and

calculating the time required to remove the second amount of the first layer of semiconductor material using the difference between the first measured conductance and the second measured conductance and a time required to complete the first etching step.

7. (Original) The method of Claim 1 the method comprising:

repeating steps (d) through (f) to identify an optimum etch depth for the first layer of semiconductor material.

8. (Original) The method of Claim 1 wherein the first layer of semiconductor material includes a first conductivity type and the second layer of semiconductor material includes a second conductivity type different from the first conductivity type.

9. (Original) The method of Claim 1 wherein the device is a radio frequency power device.

10. (Original) The method of Claim 1 wherein the device is a p-n junction.

11. (Original) The method of Claim 1 wherein the device is a transistor.

12. (Original) The method of Claim 1 wherein the device is a thyristor.

13. (Original) A method for precisely etching a wide bandgap semiconductor device, the method comprising the steps of:

(a) providing a multi-layer laminate including at least a first and second layer of wide bandgap semiconductor material;

(b) measuring a first conductance of the first layer of semiconductor material;

(c) first etching the first layer of semiconductor material a first amount;

(d) measuring a second conductance of the first layer of semiconductor material etched the first amount; and

(e) repeating steps (c) and (d) to determine an optimal time to etch the first layer of semiconductor material a second amount.

14. (Original) The method of Claim 13 the method comprising:

subsequent to the providing step, isolating an area of the first layer of semiconductor material for locating a conductance measurement device.

15. (Original) The method of Claim 14 wherein the step of measuring the first conductance comprises:

measuring the first conductance of the isolated area of the first layer of semiconductor material using the conductance measurement device.

16. (Original) The method of Claim 13 the method comprising:

subsequent to the repeating step, second etching the first layer of semiconductor material for the determined optimal amount of time to remove the second amount of the first layer of semiconductor material.

17. (Original) The method of Claim 16 wherein the second etching step comprises:

etching at least a portion of the first layer of semiconductor material to a junction between the first and second layer of semiconductor material.

18. (Original) The method of Claim 16 wherein the second etching step comprises:

removing at least a portion of the first layer of semiconductor material to achieve a predetermined thickness of the at least a portion of the first layer of semiconductor material.

19. (Original) The method of Claim 13 the method comprising:

determining a difference between the first measured conductance and the second measured conductance; and

calculating the optimal time using the difference between the first measured conductance and the second measured conductance and a time required to complete the first etching step.

20. (Original) The method of Claim 13 the method comprising:

repeating steps (c) and (d) to identify an optimum etch depth for the first layer of semiconductor material.

21. (Original) The method of Claim 13 wherein the first layer of semiconductor material includes a first conductivity type and the second layer of semiconductor material includes a second conductivity type different from the first conductivity type.

22. (Original) The method of Claim 13 wherein the device is a radio frequency power device.

23. (Original) The method of Claim 13 wherein the device is a p-n junction.

24. (Original) The method of Claim 13 wherein the device is a transistor.

25. (Original) The method of Claim 13 wherein the device is a thyristor.

26. (Amended) A method for use in semiconductor fabrication comprising:

establishing a mathematical correlation for determining an etch time for etching a material, the mathematical correlation reflecting a relationship between a conductance of a layer of said material and a thickness of said layer, wherein said layer conductance reduces with etching of said layer thickness; ~~and~~

using the mathematical correlation to determine an etch time for etching an amount of the material~~.~~; and

using said determined etch time to produce a multi-layer laminate including at least a first and second layer of wide bandgap semiconductor material.

27. (Amended) A method for use in semiconductor fabrication comprising:

establishing a mathematical correlation for determining an etch time for etching a material, the mathematical correlation reflecting a relationship between a conductance of a layer of said material and a thickness of said layer, wherein said layer conductance reduces with said layer thickness; and

using the mathematical correlation to determine an etch time for etching an amount of the material,

wherein said step of establishing comprises

(a) obtaining a first conductance measurement of a layer and a second conductance measurement of the layer, wherein the first conductance measurement of the layer is obtained before an etch of the layer and the second conductance measurement of the layer is obtained after the etch of the layer; and

(b) using the first conductance measurement of the layer and the second conductance measurement of the layer to determine the etch time for etching an additional amount of the layer of material.

28. (Previously Added) The method of Claim 27 comprising:

repeating steps (a) and (b) to achieve an optimum etch depth for the layer of material.

29. (Cancelled)

30. (Previously Added) The method of Claim 26 wherein an initial layer thickness remains unknown.